REMARKS

This is in response to the Office Action mailed on January 9, 2004.

Claims 1, 4, 6, 9, 11, 15, 18, 20, 22, 24, 26, 29, and 31 are amended, claim 16 is canceled; as a result, claims 1, 2, 4-15, and 17-40 are now pending in this application.

Reservation of the Right to Swear Behind References

Applicant maintains the right to swear behind any references which are cited in a rejection under 35 U.S.C. §§102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited references are not to be interpreted as admissions that the references are prior art.

§103 Rejection of the Claims

Claims 1, 2, and 4-40 were rejected under 35 USC § 103(a) as being unpatentable over Dye (U.S. Patent No. 6,145,069).

Applicant respectfully traverses.

The claims of the present invention recite, among other things, a volatile memory, a cache memory, and a compression and decompression engine connected to the volatile memory and the cache memory. The claims of the present invention further recite that the volatile memory, the cache memory, and the compression and decompression engine are located in a single chip.

For example, claim 1 recites:

a volatile main memory;
a cache memory connected to the volatile main memory; and
a compression and decompression engine connected between the volatile main memory and the cache memory, wherein the volatile main memory, the cache memory, and the compression and decompression engine are located in a single chip.

Dye discloses a system having a flash memory located in one chip and a compression and decompression engine located in another chip. Flash memory is a non-volatile memory.

The Office Action indicates that

"it is common knowledge that volatile memory (RAM/DRAM) can be substituted for non-volatile memory when it is not desired/required to retain data upon power loss and when cost is an issue because flash memories are more expensive than RAM/DRAM (this is recognized by Dye; 1/30-37)."

The Office Action further indicates that

"Flash memory is mainly used where data non-volatility is required by the system. Thus, it is would have been obvious to substitute [[non]]volatile memory for the flash memory of Dye when data non-volatility and memory cost are not required by the system."

Regarding the substitution of volatile memory for non-volatile memory:

Applicant understands the indication in the Office Action that volatile memory (RAM/DRAM) can be substituted for non-volatile memory when it is not desired/required to retain data upon power loss. However, Applicant submits that indication in the Office Action may not apply to Dye to support the obviousness rejection because Applicant is unable to find in Dye any teaching or suggestion about substituting volatile memory for the flash (non-volatile) memory in the Dye's system. Further, even if a person tried to practice the Dye's system using the substituted volatile memory instead of the flash memory taught by Dye, the function of the Dye's system would be destroyed because the volatile memory would lose all stored data when power is cut off from the Dye's system. Thus, notwithstanding that substituting volatile memory for the flash memory in the Dye's system is not obvious, substituting volatile memory for the flash memory in the Dye's system also destroys the function of the Dye's system.

Regarding the combination of data non-volatile memory and cost:

Applicant also understands the indication in the Office Action that volatile memory can be substituted for flash memory when data non-volatile and cost are not required by the system. As indicated in the Office Action, Dye recognizes that the cost per bit of flash memory exceeds that of volatile memory (Dye, column 1, lines 30-37). Applicant submits that the combination of data non-volatility and cost may also not apply to Dye to support the obviousness rejection. Applicant submits that since Dye recognizes that the cost per bit of flash memory exceeds that of volatile memory, Dye would have taught or suggested about substituting volatile memory for the flash memory in the Dye's system to reduce cost. However, Applicant is unable to find in Dye any teaching or suggestion of substituting volatile memory for the flash memory in the Dye's

system when data non-volatile and cost are not required by the system. Even if a person tried to reduce the cost by substituting volatile memory for the flash memory while practicing the Dye's system, the function of the Dye's system would be destroyed as explained above.

Regarding the combination of the volatile memory and the compression and decompression engine:

As shown in the example of claim 1, the claims of the invention also recites a, among other things, a compression and decompression engine connected to a volatile memory. Applicant is unable to find in Dye any teaching or suggestion about the *combination* of a compression and decompression engine connected to the volatile memory. Therefore, Applicant believes that the combination of the compression and decompression engine connected to the volatile memory is not obvious over Dye.

Regarding the single chip:

The Office Action agrees that Dye does not specifically teach a single chip having the main memory, buffer, cache memory, and compression and decompression engine. The Office Action, however, cites In re Larson 144 USPQ 347 (CCPA 1965) and In re Tomoyuki Kohno 157 USPQ 275 (CCPA 1968) to point out that "to make integral is not generally given patentable weight."

Applicant submits that the Larson and Tomoyuki Kohno cases may not apply to the current application for the reasons explained below.

In re Larson, the courts affirmed the rejection holding that the use of one piece construction instead of the separate pieces disclosed in a prior art is matter of obvious engineering choice. In re Tomoyuki Kohno, the courts affirmed the rejection holding that modifying a part among parts of a structure disclosed in a first prior art in view of a second prior art to make all the parts integrally formed in one piece is an obvious modification.

Applicant submits that the present invention is different from both of the In re Larson case and the In re Tomoyuki Kohno case because integrating or combining the elements of the present invention into a single chip is neither an obvious engineering choice as compared to In re Larson case nor an obvious modification as compared to the In re Tomoyuki Kohno case.

For instance, in some situations, it might not be practicable to combine a volatile memory and a compression and decompression engine into a single chip because the compression and decompression engine may introduce data access latency. The inventor of the present invention, however, found a practicable way to combine the compression and decompression engine with the volatile main memory in the same chip by way of combining the compression and decompression engine, the volatile main memory, and the cache memory in a single chip. By combining the compression and decompression engine, the volatile main memory, and the cache memory in a single chip, data access latency of the compression and decompression engine would be hidden or compensated by the cache memory.

Based on the reasons explained above, integrating or combining the compression and decompression engine with the volatile main memory and the cache memory in a single chip, as claimed in the present invention, is neither an obvious engineering choice nor an obvious modification.

Regarding the Official Notice:

The Office Action also indicates that

"It is well-known in the arts to integrate components onto a single chip to decrease distance between elements and allows for faster access, decreasing the size of the overall system space and power requirements. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to integrate the main memory, buffer, cache memory, and compression and decompression engine on a single chip to provide for a faster, smaller, and less expensive system."

Applicant respectfully traverses the rejection supported by the portion of the Office Action indicated above. Portion of the Office Action above indicates that it would have been obvious to one having ordinary skill in the art at the time the invention was made to integrate the main memory, buffer, cache memory, and compression and decompression engine on a single chip to provide for a faster, smaller, and less expensive system. However, the Office Action offers no supporting documents in rejecting the recited elements of the claims such as the volatile main memory, the cache memory, and the compression and decompression engine in which these elements are "located in a single chip". Thus, Applicant assumes that the Examiner is taking Official Notice in rejecting the volatile main memory, the cache memory, and the compression and decompression engine in which these elements are "located in a single chip".

Applicant respectfully objects to the taking of Official Notice with a single reference obviousness rejection and, pursuant to M.P.E.P. § 2144.03, Applicant respectfully traverses the assertion of Official Notice and requests that the Examiner cite documents to support the rejection that the volatile main memory, the cache memory, and the compression and decompression engine in which these elements being "located in a single chip" is obvious.

All of the above reasons demonstrate that the claims of the present invention are not obvious over Dye. Accordingly, Applicant requests that the rejection of claims 1, 2, 4-15, and 17-40 reconsidered and withdrawn.

Regarding the currently amended claims:

Although Applicant believes that the claims of the present invention are not obvious over Dye, Applicant amended independent claims 1, 4, 6, 9, 11, 15, 18, 20, 22, 24, 26, 29, and 31 to expedite the prosecution of this patent application.

Regarding claim 1, Applicant is unable to find in Dye "a plurality of static registers connected to the volatile main memory" and "a plurality of register controllers, each of the register controllers being connected to one of the static registers". Therefore, Applicant requests that the rejection of claim 1 be reconsidered and withdrawn and that claim 1 and dependent claims of claim 1 be allowed.

Regarding claim 4, Applicant is unable to find in Dye "a static memory having a plurality of static registers connected to the dynamic memory" and "a plurality of register controllers, each of the register controllers being connected to one of the static registers". Therefore, Applicant requests that the rejection of claim 4 be reconsidered and withdrawn and that claim 4 and dependent claims of claim 4 be allowed.

Regarding claim 6, Applicant is unable to find in Dye "a cache memory having a plurality of static registers" and "a plurality of register controllers, each of the register controllers being connected to one of the static registers". Therefore, Applicant requests that the rejection of claim 6 be reconsidered and withdrawn and that claim 6 and dependent claims of claim 6 be allowed.

Regarding claim 9, Applicant is unable to find in Dye "a plurality of static registers connected to the volatile main memory" and "a plurality of register controllers, each of the

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register controllers being connected to one of the static registers". Therefore, Applicant requests that the rejection of claim 9 be reconsidered and withdrawn and that claim 9 and dependent claims of claim 9 be allowed.

Regarding claim 11, Applicant is unable to find in Dye "a cache memory having a plurality of static registers" and "a plurality of register controllers, each of the register controllers being connected to one of the static registers". Therefore, Applicant requests that the rejection of claim 11 be reconsidered and withdrawn and that claim 11 and dependent claims of claim 11 be allowed.

Regarding claim 15, Applicant is unable to find in Dye "placing a plurality of static registers between on a data path between an input/output buffer and the compression and decompression engine" and "connecting a plurality of register controllers to the static registers to control the static registers, wherein each of the register controllers is connected to one of the static registers". Therefore, Applicant requests that the rejection of claim 15 be reconsidered and withdrawn and that claim 15 and dependent claims of claim 15 be allowed.

Regarding claim 18, Applicant is unable to find in Dye "receiving input data at a plurality of static registers of a cache memory" and "controlling the plurality of static registers with a plurality of register controllers, wherein each of the static registers is controlled by one of the register controllers". Therefore, Applicant requests that the rejection of claim 18 be reconsidered and withdrawn and that claim 18 and dependent claims of claim 18 be allowed.

Regarding claim 20, Applicant is unable to find in Dye "processing the data at a plurality of static registers of a cache memory to produce processed data" and "controlling the plurality of static registers with a plurality of register controllers, wherein each of the static registers is controlled by one of the register controllers". Therefore, Applicant requests that the rejection of claim 20 be reconsidered and withdrawn and that claim 20 and dependent claims of claim 20 be allowed.

Regarding claim 22, Applicant is unable to find in Dye "a static memory having a plurality of static registers" and "a plurality of register controllers, each of the register controllers being connected to one of the static registers". Therefore, Applicant requests that the rejection of claim 22 be reconsidered and withdrawn and that claim 22 and dependent claims of claim 22 be allowed.

Regarding claim 24, Applicant is unable to find in Dye "a plurality of static registers" and "a plurality of register controllers, each of the register controllers being connected to one of the static registers". Therefore, Applicant requests that the rejection of claim 24 be reconsidered and withdrawn and that claim 24 and dependent claims of claim 24 be allowed.

Regarding claim 26, Applicant is unable to find in Dye "a static memory block having a plurality of static registers" and "a plurality of register controllers, each of the register controllers being connected to one of the static registers". Therefore, Applicant requests that the rejection of claim 26 be reconsidered and withdrawn and that claim 26 and dependent claims of claim 26 be allowed.

Regarding claim 29, Applicant is unable to find in Dye "passing the input data through a plurality of static registers" and "controlling the plurality of static registers with a plurality of register controllers, wherein each of the static registers is controlled by one of the register controllers". Therefore, Applicant requests that the rejection of claim 29 be reconsidered and withdrawn and that claim 29 and dependent claims of claim 29 be allowed.

Regarding claim 31, Applicant is unable to find in Dye "receiving input data at a plurality of static registers of a static memory block" and "controlling the plurality of static registers with a plurality of register controllers, wherein each of the static registers is controlled by one of the register controllers". Therefore, Applicant requests that the rejection of claim 31 be reconsidered and withdrawn and that claim 31 and dependent claims of claim 31 be allowed.

Regarding the previously presented claims:

Claim 33, as previously presented, recites:

    a dynamic memory;
    a plurality of static registers connected to the dynamic memory;
    a plurality of register controllers, each of the register controllers being connected to one of the static registers;
    a compression and decompression engine connected to the dynamic memory and the plurality of static registers; and
    an error detection and correction engine connected to the dynamic memory and the compression and decompression engine, wherein the dynamic memory, the plurality of static registers, the plurality of register controllers, the compression and decompression engine, and the error detection and correction engine are located in a single chip.

Applicant is unable to find in Dye "a plurality of static registers connected to the dynamic memory" and "a plurality of register controllers, each of the register controllers being connected to one of the static registers". Therefore, Applicant requests that the rejection of claim 33 be reconsidered and withdrawn and that claim 33 and dependent claims of claim 33 be allowed.

Claim 36, as previously presented, recites:

a processor; and
a memory device connected to the processor, the memory device including:
    a dynamic memory;
    a plurality of static registers connected to the dynamic memory;
    a plurality of register controllers, each of the register controllers being connected to one of the static registers;
        a compression and decompression engine connected to the dynamic memory and the plurality of static registers; and
        an error detection and correction engine connected to the dynamic memory and the compression and decompression engine, wherein the dynamic memory, the plurality of static registers, the plurality of register controllers, the compression and decompression engine, and the error detection and correction engine are located in a single chip.

Applicant is unable to find in Dye "a plurality of static registers connected to the dynamic memory" and "a plurality of register controllers, each of the register controllers being connected to one of the static registers". Therefore, Applicant requests that the rejection of claim 36 be reconsidered and withdrawn and that claim 36 and dependent claims of claim 36 be allowed.

Claim 39, as previously presented, recites:

transferring input data to a plurality of static registers;
independently controlling the transferring of the input data at each of the static registers;
compressing the input data to produce compressed data;
storing the compressed data into a dynamic memory;
reading the compressed data from the dynamic memory; and
decompressing the compressed data, wherein transferring, controlling, compressing, storing, reading, and decompressing are performed on a single chip.

Applicant is unable to find in Dye "transferring input data to a plurality of static registers" and "independently controlling the transferring of the input data at each of the static registers". Therefore, Applicant requests that the rejection of claim 39 be reconsidered and withdrawn and that claim 39 and dependent claims of claim 39 be allowed.

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CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative at (612) 373-6969 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this __9__ day of June, 2004.

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